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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,009	11/26/2003	Jurgen Lindolf	INFN/0040	7545

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,009	LINDOLF ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003 and 12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *1-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/12/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 10/12/2004 is acceptable.

Claim Objections

2. **Claim 1** is objected to because of the following informalities: Claim 1 recites "an antifuse structure in a substrate comprising: forming a conductive region on the substrate". However, it is clear that the conductive region (1) is in the substrate as evident by, as an example, paragraphs [0009] and [0021] and the figures of the present invention and as will be clearly detailed below concerning claim 5. Similarly, the nonconductive region (2) should also be in the substrate. Appropriate correction is required.

Claims 2-9 are objected to because they depend on objected claim 1.

For examination purpose, the limitation "forming a conductive region on the substrate" is treated as "forming a conductive region **in** the substrate" and "forming a nonconductive region adjoining the conductive region on the substrate" is treated as "forming a nonconductive region adjoining the conductive region **in** the substrate".

Claim Rejections - 35 USC § 102 and/or § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in
>
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-15 and 17-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Bertin et al. U.S. Patent 6,812,122.

Bertin discloses in Figure 2A and respective portions of the specification a method for producing an antifuse structure in a substrate, the resulting antifuse, and an inherent method of using the antifuse as claimed.

Referring to **claims 1, 10, and 14**, Bertin discloses a method for producing an antifuse structure in a substrate, comprising:

forming a conductive region (204) in the substrate (202), the conductive region defining a first upper surface (206) and a first lateral boundary surface (210) which meet at an angle (generally referred to as 218) to form an edge;

forming a nonconductive region (212/214) adjoining the conductive region in the substrate, the nonconductive region defining a second upper surface and a second lateral boundary surface (210); wherein the first and second lateral boundary surfaces (210) are in facing relationship and form an interface (generally referred to as 210); and

forming a dielectric layer (216) over at least a portion of the first upper surface of the conductive region and at least a portion of the edge, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer (generally indicated by path 226, column 7, lines 37-50).

Referring to **claims 2, 13, and 14**, Bertin further discloses forming a conductor (220) on the dielectric layer (216).

Referring to **claims 3, 11, and 15**, Bertin further discloses that the conductive region (204) defines a comer (generally referred to as 218) and wherein forming the dielectric layer (216) comprises forming the dielectric layer over the comer. Referring to the limitation "area of relatively increased field strength" of claim 11, the area of relatively increased field strength results in, as cited above, the breakdown of the dielectric layer 216/212 at "the merge" indicated generally as 218 and the eventual path indicated as 226).

Referring to **claim 4**, Bertin further discloses that the first lateral boundary surface (210) is substantially orthogonal to a lower surface (generally indicated as 206) of the dielectric layer (216) interfacing with the edge.

Referring to **claim 5**, Bertin further discloses that the conductive region (204) is a doped semiconductor region (n+). Note also that this limitation amplifies the fact that the inventive conductive region 1 and the nonconductive region 2 of the present invention are formed *in* the substrate, unless the substrate is a supporting substrate, in which case, the resulting antifuse is not in the substrate, but is on the substrate, and in which case, the detailed description of the present invention and the figures shall also be described accordingly.

Referring to **claims 6-8 and 18-20**, Bertin further discloses that the nonconductive region (212/214) comprises at least one of SiO_2 and SiN (column 6, lines 40-52) and the dielectric layer (216) comprises SiN (column 6, lines 53-55).

Referring to **claims 9, 12, and 17**, Bertin further discloses that the dielectric layer (216) is disposed over at least a portion (a portion of portion 212 or as aptly termed the "merge area" by Bertin) of the nonconductive region (212/214).

4. **Claims 10-20** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Takagi et al. U.S. Patent 5,625,219.

Takagi discloses in Figures 1-6 and respective portions of the specification an antifuse and an inherent method of using the antifuse as claimed or substantially as claimed depending on how broad one in the art interprets "region" and "layer".

Specifically, Takagi discloses a single region 7 that is functionally equivalent to the nonconductive region 2 and the dielectric layer 4 of the present invention. More specifically and with reference to Figs. 5C and 6, with added reference characters as depicted on the following page for ease of explanation, and referring to **claims 10, 13, and 14**, Takagi discloses an antifuse, comprising:

a first conductive region (62), the first conductive region defining a first upper surface (62US) and a first lateral boundary surface (SS) which meet at an angle (62C) to form an edge;

a nonconductive region (7B) adjoining the first conductive region (62), the nonconductive region defining a second upper surface and a second lateral boundary surface

(SS); wherein the first and second lateral boundary surfaces are in facing relationship and form an interface (generally indicated as SS);

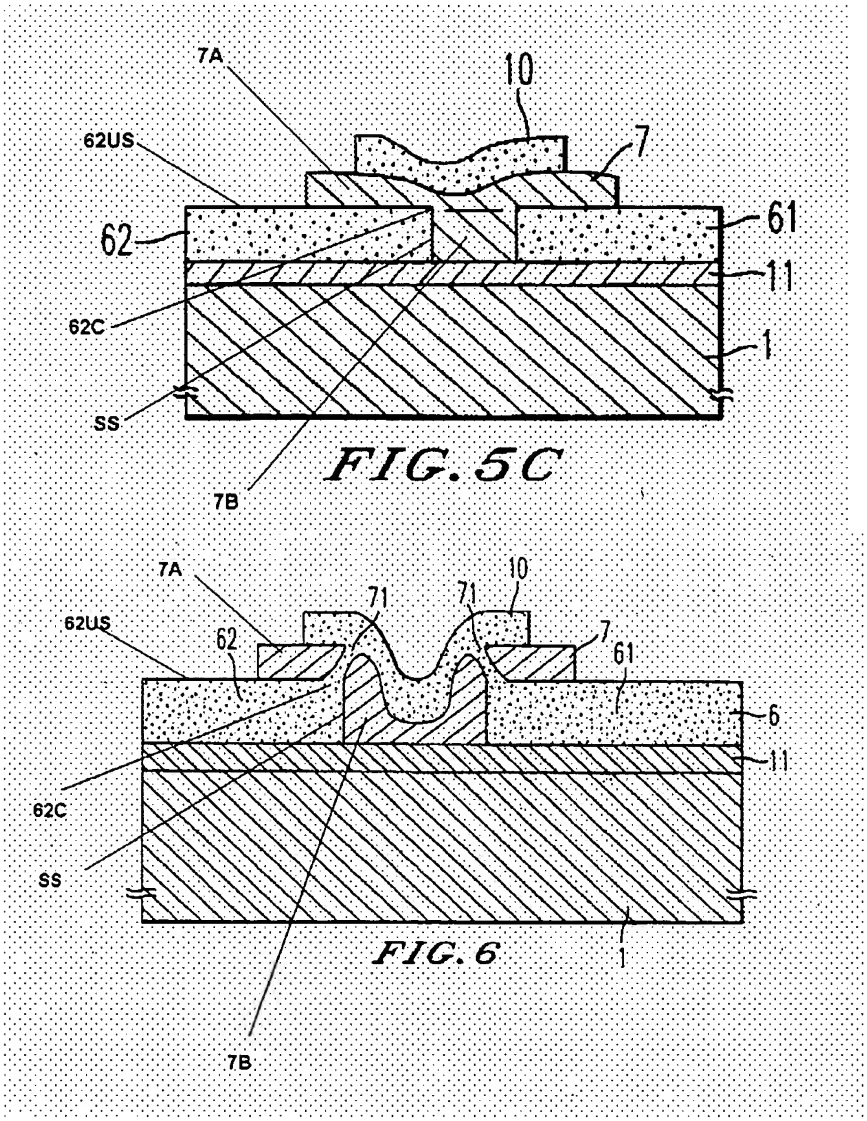

FIG. 5C

FIG. 6

a dielectric layer (7A) disposed over at least a portion of the first upper surface (62US) of the first conductive region and at least a portion of the edge (62C), whereby an area of relatively increased field strength is produced during application of a programming voltage to form a

breakdown channel (71) in the dielectric layer; and a second conductive region (10) on the dielectric layer.

Referring to **claims 11 and 15**, Takagi further discloses that the conductive region (62) defines a comer (62C) and wherein forming the dielectric layer (7A) comprises forming the dielectric layer over the comer. Referring to the limitation "area of relatively increased field strength" of claim 11, the area of relatively increased field strength results in the breakdown of the dielectric layer 7A at the corner and the eventual forming of the path 71).

Referring to **claims 12 and 17**, Takagi further discloses that the dielectric layer (7A) is disposed over at least a portion of the nonconductive region (7B, best seen in Fig. 5C).

Referring to **claim 16**, Takagi further discloses that the first conductive region (62) and the nonconductive region (7B) form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer (7A, best seen in Fig. 5C).

Referring to **claims 18-20**, Takagi further discloses that the nonconductive region (7B) comprises SiN and the dielectric layer (7A) comprises SiN (column 6, lines 61-63).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
November 13, 2004